Hrit Mukherjee

Email: hritmukherjee@gmail.com

*A **circuit designing enthusiast**, highly passionate about **Analog/Mixed Signal Design,** and particularly interested in the research and development of high speed, high precision Electronics devices.*

Academic Background

2021	Bachelor of Engineering (Electronics and Telecommunication, Hons) Jadavpur University, Kolkata, India. **CGPA:- 9.6** **Dept. Rank: 4** **Final Year Project Advisor: Dr. Mrinal Kanti Naskar**
2017	Higher/Senior Secondary Examination Nava Nalanda High School (affiliated to West Bengal Council of Higher Secondary Education), Kolkata, India. **Percentage: 96.40%** **State Rank: 8**
2015	Secondary Examination Nava Nalanda High School (affiliated to West Bengal Council of Secondary Education), Kolkata, India. **Percentage: 94.00%** **Percentage (Science Group): 99.67%**

Interests

Analog and Mixed Signal Circuit Design, Microelectronics and Device physics, Digital Signal Processing, Embedded Systems.

Work Experience

1. **Analog Design Engineer, Texas Instruments**, Bangalore, India (Dec'21 – present)
   Project: **DISHA (4th order Continuous Time Sigma Delta ADC).** Team: Precision ADC, High Speed Converters.
   - Contributed to ADCTOP level architecture design and modelling based on SNR and Linearity requirements. (Key Specs: 122dB SQNR with 125dB THD for signal bandwidth upto 1MHz at 64MSPS clock with inherent anti-aliasing-> improvement over **ADI's adaq7768 and ad7768** family)
   - Designed a 3-stage differential input differential output miller compensated summing amplifier. (Key Specs: Achieved 170MHz UGB, 46° PM, 9dB GM, 80dB DC gain at 1.1 mA current consumption from 1.8V supply, has 8ns settling time supporting a 4-bit SAR ADC load)
   - Designed a 4-bit SAR ADC. (Key Specs: Achieved 6ns Conversion Time with 8bits accuracy supporting Main DAC, Compensation DACs and ADC DIGITAL TOP -> improvement over **TI's ads921x family**).
   - Designed 2 4-bit R-DACs. (Key Specs: Achieved 5bits settling with 95dB linearity at the output).
2. **Analog Design Engineer, Cirel Systems**, Bangalore, India (Jul'21 – Nov'21)
   Project: **KALAMOS Stylus IC.** Team: Design Team
   - Designed a Charger powered by SuperCAP or Li-ion battery. (Key Specs: Delivers a charging current from 21uA to 4.2mA or 1mA to 200mA with 10% accuracy.)
   - Designed an LDO Powered by SuperCap or Li-ion battery. (Key Specs: Soft starts upto 1.6V, delivers a load of 0 to 100mA at 1.8V output with input varying from 2.5V to 5.5V.)
3. **Summer Intern, Variable Energy Cyclotron Center (VECC),** Kolkata, India (May'19 – July'19)
   Project: Low Power High Speed High Resolution DAC design. Team: ASIC Team
   - Designed a Low Power High Speed High Resolution 9-bit DAC. The proposed architecture was designed following current steering architecture, having a combination of a 6-bit fine and a 3-bit coarse DAC, whose individual responses were added using a non-inverting opamp.

   Project Report: https://hrit-mukherjee.github.io/Project%20Report.pdf

Skillsets

1. Programming: C, C++, Python, Matlab, Simulink.
2. Operating Systems: Windows, Linux.
3. Simulators: Cadence, LT Spice, P Spice, T Spice, Circuit Maker, Xilinx, Vivado, TCAD Silvaco.
4. Embedded System Platforms: Arduino UNO, NodeMCU, RaspberryPi 3.
5. Typesetting tools and version control: Latex, Git & Github.

Relevant course-works done

1. **Razavi Electronics 1** – by Behzad Razavi, University of California, Los Angeles.
2. **Engineering Electronics II and Analog IC Design (Spring, 2019)** - by R. Jacob Baker, PhD, PE, University of Nevada, Las Vegas.
3. **Analog Circuits** and **IC Design –** by Dr. Nagendra Krishnapura, ECE, IIT Madras.
4. **VLSI Data Conversion Circuits –** by Dr. Shanthi Pavan, EE, IIT Madras.
5. **Digital logic circuits** and **systems, Digital Signal Processing**, Professor Dr. Mrinal Kanti Naskar, Dept. of ETCE, JU.

Publications

1. H. Mukherjee, M. Kar, and A. Kundu, **Enhancement in analog/RF and power performance of underlapped dual-gate GaN-based MOSHEMTs with quaternary InAlGaN barrier of varying widths.** *J. Electron. Mater.* 51, 692–703 (2021).

2. H. Mukherjee, R. Dasgupta, M. Kar and A. Kundu, **A comparative analysis of analog performances of underlapped dual gate AlGaN/GaN based MOS-HEMT and Schottky-HEMT**, in *IEEE Calcutta Conference (CALCON)*, Kolkata, p. 412 (2020).

3. S. Ghosh, G. Bagla, H. Mukherjee, M. Kar, and A. Kundu, **Impact of Mole Fraction Variation on the Analog/RF Performance of Quaternary InAlGaN DG MOS-HEMTs.** *J. Electron. Mater.* 51, 692–703 (2021).

4. P. Roy, H. Mukherjee, M. Kar, S. Chatterjee and A. Kundu, **Comparative study on Analog & RF Performance of an Underlapped DG InAlGaN/GaN based MOS-HEMT between GaN layer width and InAlGaN layer width variation**, 2023 IEEE 2nd International Conference on Industrial Electronics: Developments & Applications (ICIDeA), Imphal, India, 2023, pp. 64-69.

5. K. Sorkhel, A. Ghosh, H. Mukherjee, S. Chatterjee, M. Kar and A. Kundu, **Analytical Comparison of Analog/RF Performance of DG InAlGaN/GaN based MOS-HEMTsfor GaN width variation**, *2023 IEEE 2nd International Conference on Industrial Electronics: Developments & Applications (ICIDeA)*, Imphal, India, 2023, pp. 54-59.

Projects

1. Hardware Implementation of Direction of Arrival (DoA) estimation and Node Localization algorithm for Smart Antenna in Wireless Sensor Networks

- *Research project under the guidance of* ***Prof. Dr. Mrinal Kanti Naskar****, Dept. of ETCE, Jadavpur University* (August'20-May'21) (Final Year Project.pdf (hrit-mukherjee.github.io))

- ***Final Year Project, Jadavpur University***

2. Analytical Modeling of Surface Potential and Threshold Voltage for small geometry MOSFETs, HEMTs and FinFETs with non-uniformly doped channels

- *Research project under the guidance of* ***Prof. Dr. Amitava Dasgupta****, Dept. of EE, IIT Madras* (April'20-July'20)

- ***Summer Internship, Microelectronics and MEMS Laboratory Group, IIT Madras.***

3. Hurry-Cane: See through my eyes – IoT based electronic stick aimed to provide artificial vision to the visually impaired people by facilitating in their safe and independent terrestrial locomotion by virtue of its applications.

- *Research project under the guidance* ***of Prof. Dr. Sayan Chatterjee****, Dept. of ETCE, Jadavpur University* (Feb'20-Dec'20) (https://github.com/Hurry-Cane/Papier_Submission/blob/master/Hurry-Cane.pdf)

- ***Research Project, TEQIP PHASE-III, Jadavpur University.***

Awards and Achievements

1. Recipient of **2021 IEEE Eelctron Device Society Undergraduate Student Scholarship** (Region 10).
2. 1st Runner-up, **Anveshan 2019-20: Student Research Convention**, Social Science Category, a national level research contest, organized by AIU (Association of Indian Universities).
3. 2nd Runner-up, **Electroniche**(a competitive event involving circuit solving, designing and simulating circuits based on given specifications), organized by Srijan'19 (technological fest of Jadavpur University).
4. Winner (multiple times) of **DhrisTI** online contest (on analog and microcontrollers), organized by Texas Instruments.
5. Ranked 202 in **WBJEE** (West Bengal Joint Entrance Examination), 2017.
6. Secured 8th position in in **Higher Secondary Examination**, 2017.

Responsibilities Holding / Held

1. **IEEE** *Student Member, Kolkata Section*
   - Member of the Management team of Jadavpur University Student Branch of IEEE, Kolkata Section.
   - Member of IEEE EDS, Region 10.
2. Mentor for **Texas Instruments** Analog Foundations Bootcamp program for New College Graduates.
3. Coordinator for **Jadavpur University Code Club** and **Jadavpur University Science Club**.
4. Executive committee member for **Srijan-Technological fest of Jadavpur University**.

Referees

- **Dr. Mrinal Kanti Naskar –** Professor
  Department of ETCE, Jadavpur University
  Email: mrinaletce@gmail.com
- **Rahul Sharma –** Analog Design Manager
  Precision ADC Team, Analog Signal Chain, Texas Instruments
  Email: A0131586@ti.com